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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/018,762 | 04/18/2002 | Ian J Forster | P/61728-PCT | 2649 |

156 7590 08/11/2004
KIRSCHSTEIN, OTTINGER, ISRAEL
& SCHIFFMILLER, P.C.
489 FIFTH AVENUE
NEW YORK, NY 10017

EXAMINER

JACKSON, BLANE J

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2685

DATE MAILED: 08/11/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Office Action Summary

Application No.

10/018,762

Applicant(s)

FORSTER ET AL.

Examiner

Blane J Jackson

Art Unit

2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 April 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-21, 23, 25 and 27-36 is/are rejected.
- 7) ☒ Claim(s) 22, 24 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 19-21, 23, 25 and 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camiade et al. (U.S. Patent 5,305,469).

As to claims 19, 20, 25 and 36, Camiade teaches an amplitude modulation (modem) receiver and method for receiving an input signal and generating a corresponding demodulated signal comprising:

A transistor biased to be operable as a reflection amplifier for reflectively amplifying the input signal or as a detector for detecting an amplified input signal to generate the demodulated signal (figure 4: a circuit to select a AM detector or reflection amplifier mode based on the biasing of the FET gate voltage, source and drain currents as made clear in figure 2, column 2, line 45 to column 3, line 11).

Camiade also teaches that it is possible to carry out AM, PM or frequency modulation (FM) depending on the way in which the reflection amplifier is used (column 2, lines 54-57).

Camiade does not teach a *transistor biased to be simultaneously operable as a reflection amplifier and amplitude modulation (AM) detector*. However it is well known in

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the art to bias a transistor to achieve class A, B or C type transistor circuit with a large degree of non-linearity expected at class C, class A classified as a linear amplifier or operation region and class B as a compromise of class A and C for specific performance related to power consumption, mixing, harmonic generation and amplification. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to bias the circuit of Camiade like a class B amplifier to obtain a circuit exhibiting both detection and amplification characteristics from a single active transistor.

As to claim 21, Camiade modified teaches the receiver according to claim 20 wherein the transistor is operable to conduct a current therethrough in a range of 5uA to 110uA to function in the non linear region (actual biasing values in the non linear region are expectedly low where the actual values depend on the selected transistor, column 4, lines 61-68).

As to claim 23, Camiade teaches an antenna assembly for receiving input radiation and generating therefrom the input signal for the transistor (figure 4, antenna (9) and matching circuits (12), column 5, lines 43-45).

As to claims 31-35, Camiade specifically teaches an identification tag comprising:

A modulation receiver for receiving an input signal and generating a corresponding demodulated signal including a transistor biased to be operable as a

reflection amplifier for reflectively amplifying the input signal or as a detector for detecting an amplified input signal to generate the demodulated signal, the modulation receiver being operable to be responsive to radio radiation received thereat (figure 4: specifically a modem circuit switched as an AM detector for receiver circuits or as a reflection amplifier for application as a badge/ transponder, based on the biasing of the FET gate voltage, source and drain currents as made clear in figure 2, column 2, line 45 to column 3, line 11).

Camiade does not teach a *transistor biased to be simultaneously* operable as a reflection amplifier and amplitude modulation (AM) detector. However it is well known in the art to bias a transistor to achieve class A, B or C type transistor circuit with a large degree of non-linearity expected at class C, class A classified as a linear amplifier or operation region and class B as a compromise of class A and C for specific performance related to power consumption, mixing, harmonic generation and amplification. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to bias the circuit of Camiade like a class B amplifier to obtain a circuit exhibiting both detection and amplification characteristics from a single active transistor.

Allowable Subject Matter

2. Claims 22, 24 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wollesen (U.S. Patent 3,510,781) discloses an early discussion of an autodyne converter using a field effect transistor operating in the non-linear region.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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